



Selection of Mode S Messages Using FPGA

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Abstract:

Currently, there is a great evolution in the use of Mode S in air traffic. Simultaneously with the development of electronics, it is possible to use the FPGA (Field Programmable Gate Arrays). To address this challenge, Mode S messages selector has been designed to select Mode S questions and answers from the whole spectrum of signals captured by the receiver AOR AR 5000 A.

Keywords:

DF 18, Extended squitter, FPGA, Mode S, selector, SQB, squitter, VHDL

1. Introduction

Previous research has dealt with the equipment accuracy evaluation using the Mode S position location data. This evaluation was carried out by commercial Mode S receiver. Such a receiver can be constructed using the principle of FPGA. Then it is sufficient only to receive signals at a given frequency. In the first phase it is necessary to select solely Mode S messages. The Mode S messages selector supplies just this function. The Mode S messages preambles are used to distinguish questions and answers. Then it will be possible to decode these messages and subsequently to evaluate the position.

1.1. Mode S Characteristic

International Civil Aviation Organization (ICAO) has labelled the next generation of identification systems designed for worldwide air traffic control as Mode S. It was introduced mainly to solve the issue of the overloading of airspace with excessive quantities of standard SSR queries and responses in areas with heavy air traffic. This system with selective addressing is based on a network of terrestrial stations with data

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connection. Mode S is compatible with the current SSR Mode 3/A and C systems. In addition, it supports the TCAS/ACAS (Traffic Alert and Collision Avoidance System / Airborne Collision Avoidance System) systems which enables the airplanes to safely avoid collision and the ADS-B system (Automatic Dependent Surveillance-Broadcast) [1].

The Mode S system requires each interrogator to have an Identifier Code (IC) which can be carried within the uplink and downlink transmissions (1030/1090 MHz). Responding aircraft transponder identification is achieved by acquiring the unique ICAO 24-bit aircraft address. ICAO defines 25 basic message formats. Further formats can be used for individual use by different countries.

1.2. Xilinx Spartan 3™ Development Board

This board (Fig. 1) is targeted especially to support the early development and fast prototyping of small Leon based systems, computer peripherals and as general purpose FPGA development environment [2].

Although suitable for general purpose Xilinx Spartan3 FPGA developments, the incorporation of on-board volatile and nonvolatile memory, together with serial, Ethernet, video DAC, USB 2.0 and PS/2 interfaces makes this board ideal for fast prototyping, evaluation or development of software for both LEON-2 and GRLIB/LEON-3 32-bit microprocessor designs.

The board incorporates a 1.5 million gate XC3S1500 FPGA device from the Xilinx Spartan3™ family, which is supported by the free Xilinx Webpack synthesis and place and route tools. The board is provided as a kit together with a power supply, JTAG programming cable, interface cables and CD Documentation including schematics and design examples [3].



Fig. 1 Xilinx Spartan 3™ Development Board

The LEON processor is a synthesizable VHDL model of a 32-bit processor with an instruction set compatible with the IEEE-1754 (SPARC V8). The LEON processor was initially developed to provide a high performance fault-tolerant processor for space applications and is currently in use in both European and international space programs. To enable the development of system-on-a-chip (SOC) devices using the LEON core, the full VHDL source code is available both under the GNU GPL license

and under commercial licensing conditions. The Leon core is available through Hitech Global.

2. Design of Mode S Messages Selector

The Mode S messages selector is designed to select messages from the entire spectrum of the received signals. These are taken behind IF amplifier of the AR 5000 A receiver and they are fed to the A/D converter. This signal is sampled here and it is written in a single RAM. Loaded samples are being averaged which enables to create a simple digital filter. The digitized signal is brought to the threshold detector which decides whether this signal has a sufficient level or it is only noise. Pulse selector circuit follows and here it is decided whether it is Mode S signal or not. After passing through the pulse selector, signal comes to the classifier circuit. The classifier measures the pulses spacing and it distinguishes that way whether it is the mode S question or answer [4].

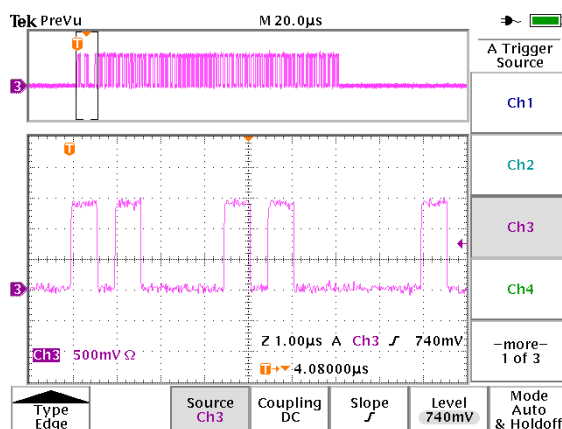


Fig. 2 Four preamble pulses in Mode S response

Question and answer differentiation of Mode S is carried out on the basis of their different preamble. The preamble of the question signal includes two pulses and the distance of their leading edges is measured. The preamble of the answer signal includes four pulses (Fig. 2) with spacing which is different from the question signal and the distance of their leading edges is measured too.

2.1. Application Testing

During test operation of the Mode S selector, problems with the pulse selector were generated. Its algorithm was initially tested on a series of pulses generated by a laboratory generator. As it was unable to generate pulses with a similar mode with sufficient accuracy, selection conditions were therefore adjusted according to the technical possibilities of the generator. When the generated signal was conformed to the conditions, the output signal was created. Two selectors for the selection of Mode S messages were necessary to be constructed due to differences in the preamble of the questions and answers, as mentioned above. Thus one selector was for the question preamble resolution and the second one for the answer preamble resolution. There was a strong bias and distortion of pulses in the preamble of incoming answer signals from

airborne transmitters (Fig. 3). Therefore, it was extremely difficult to set conditions of both selectors to correspond with the Mode S incoming signals. Therefore setting a high tolerance window of the selector was necessary. Consequently, unwanted signal pulses were loaded with the required Mode S messages [4].

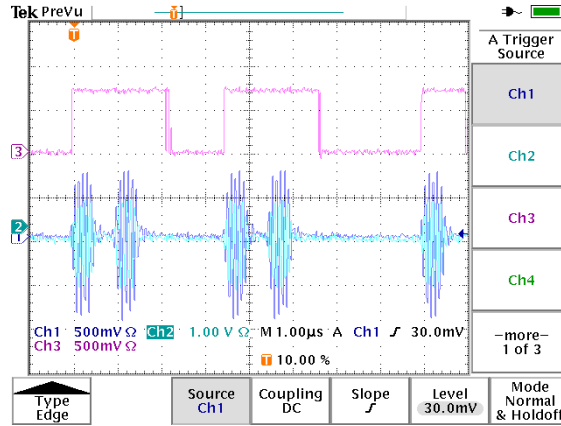


Fig. 3 Deformed pulse preamble in Mode S response

Because of this, to ensure correct function of the pulse selector, particular answer (squitter) with a sufficiently strong signal was generated. This was achieved by a Mode S mobile transmitter (Fig. 4) called SQB (Squitter Beacon). Then it was already possible to set a narrower tolerance window and to select only the impulses belonging to the mode S preamble.

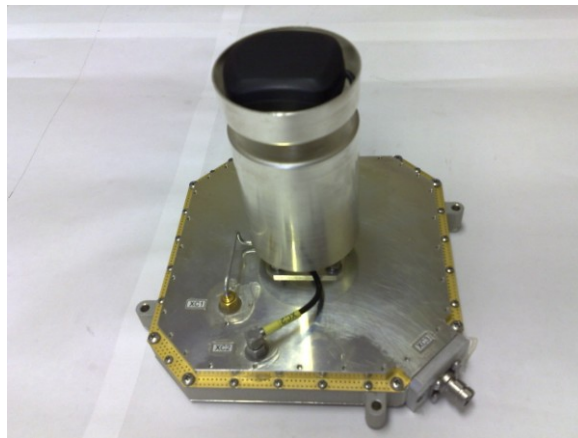


Fig. 4 Portable Squitter Beacon (SQB)

The Portable Squitter Beacon (SQB) by ERA Pardubice is smart equipment designed to support unique identification and cooperative surveillance tasks within lots of secondary surveillance functions of modern ATC. The system is specially designed to support the surveillance functions of the A-SMGCS concept and it represents a cost-effective and lightweight alternative to the usual commercial COTS transponders

employed in aeronautics. The system can be utilized widely in general aviation and can support both terminal and en-route surveillance.

The SQB is based on 1090 MHz Mode S spontaneous squitter with a unique Mode S address transmission. The Mode S address has a unique default value. The SQB operates in two available modes depending on the type of transmitted signals. The basic mode is based on the DF11 short squitter and supports all multilateration systems using 1090 MHz Mode S short squitter replies. The second mode is based on the DF18 (DF17) extended squitter designed for ADS-B applications. The SQB uses a built-in GPS receiver to provide an extended squitter message containing GPS position and identification. The SQB unit is in accordance with the ICAO Annex 10 and ICAO Manual on Mode S Specific Services recommendations.

2.2. Design of Application Program

The software part is implemented in the programming environment ISE Foundation provided by company Xilinx for its digital circuitry. The application design uses VHDL programming language, which is the same as the Verilog language used for programming the FPGA circuits [5]. In each block of the program, libraries have been defined that are used in the application. The individual inputs and outputs are defined in other parts of the program. VHDL language distinguishes several types of variables. Vectors, logical variables and whole numbers (integers) are frequently used in this proposal. Simple RAM is in the demodulation block defined as a field of integers. Whether the signal enters the block or it is out of the block or it is bidirectional, it is always defined in the header. It is also necessary to define the auxiliary signals, which then serve as a counter, an auxiliary variable, etc. The inputs and outputs of the subblocks are linked in the main block of the program. This connection can be realized in a graphical environment. Individual inputs and outputs must be assigned to the corresponding pins if the program enters block external signals such as clock frequency, the samples from the AD converter, reset signal etc.

3. Possibility of Further Targeting

It will certainly be interesting to focus on decoding the contents of the extended message Mode S (ELM) with the use of FPGAs in the next step. ELM (DF 18) broadcast in squitter also contains the positional data of the transmitting device obtained from the GPS system.

The data block is encrypted in squitter by positional pulse modulation (PPM). The data are contained in a data block that follows a four-pulse preamble [6]. So-called "Extended Squitter / Non Transponder" (ES / NT) is used for experimental purposes otherwise DF 18 message (containing BDS 05 or BDS 06 register in the field ME). DF 18 (Fig. 5) is 112-bit message format designed to broadcast extended squitter ADS-B messages from other devices than on-board transponders, where in the ME field a register carries either the ground position information (BDS 06) or it transmits information about the location of the aircraft in the air (BDS 05), if this information is available from the GPS system. Otherwise, the register contains only 56 zeros [7].

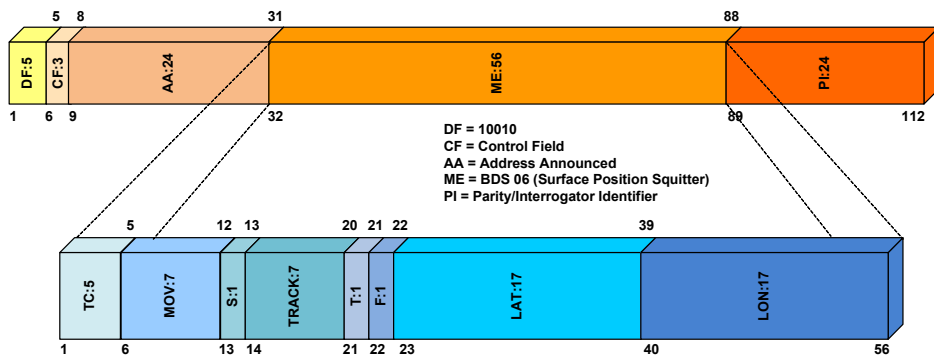


Fig. 5 Structure of the DF 18 message and ME field (BDS 06)

Different parts of 112-bit extended message DF 18 carrying data are illustrated in Fig. 6. Changing ones and zeros positions is shown in this figure too. In the position of each bit one microsecond long is a period with pulse and without pulse. In each period of DF 18 includes binary “1” of 0.5 microsecond duration represented by an impulse followed by a period without a pulse and a binary “0” represented by no pulse period followed by an impulse.

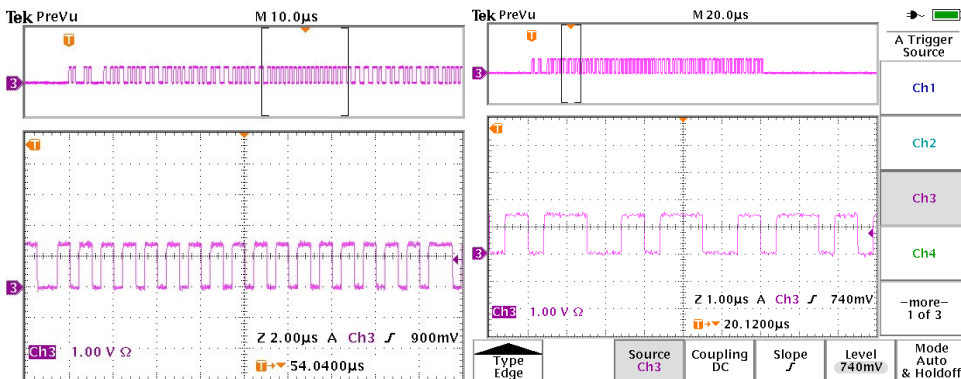


Fig. 6 DF 18 ELM details

4. Conclusion

That Mode S message selector has been developed mainly because of the possibility of the use of FPGA circuits for the selection of Mode S messages from the dense signal environment. Owing to received signal distortion this selection was very problematic and improved through the use of a mobile transmitter position data SQB, as mentioned in the article. However, the capability utilization of FPGA circuits for the selection of Mode S messages has been confirmed. The next step will be necessary to focus on improving the threshold detector circuit and then to decode the contents of the Mode S extended message (DF 17 or 18), which among others contains the positional data of the transmitting device.

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